Research of PCB Parasitic Inductance in the GaN Transistor Power Loop

Sun, Bainan; Zhang, Zhe; Andersen, Michael A. E.

Published in:
Proceedings of IEEE Workshop on Wide Bandgap Power Devices and Applications

Link to article, DOI:
10.1109/WiPDAAsia.2019.8760312

Publication date:
2019

Document Version
Peer reviewed version

Research of PCB Parasitic Inductance in the GaN Transistor Power Loop

Bainan Sun, Zhe Zhang, Michael A.E. Andersen
Department of Electrical Engineering
Technical University of Denmark
2800 Kongens Lyngby, Denmark

***Abstract*—Gallium Nitride (GaN) transistor in the high power density converter application is widely researched nowadays. High frequency switching largely reduces the volume of passive components and also leads to challenges in the PCB layout. Parasitic inductance within the critical power loop should be minimized to fully harness the potential of GaN transistor fast switching capability. This paper provides a numerical method for the power loop inductance quantification. Experimental results on the synchronous buck converter are given to validate the estimation accuracy.**

***Index Terms*—Power loop inductance, GaN transistor, finite element analysis.**

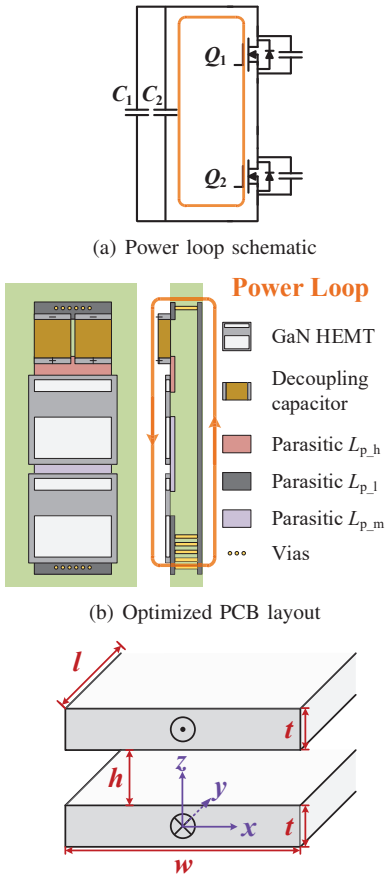
I. Introduction

GaN HEMT has lower parasitic capacitance and faster switching capability compared to its Silicon counterparts [1]–[3]. During high frequency switching, parasitic inductance of the power loop PCB tracks, as shown in Fig. 1(a), will result in drain-source voltage ringing and potentially leads to the transistor over-voltage breakdown [4]–[6]. This power loop inductance should be quantified and minimized in the design stage of PCB layout. Finite element analysis (FEA) tool is widely used and proved precise in extracting the parasitic inductance from 3D circuit models [7]–[11]. However, FEA simulation on the PCB model is time-consuming and inconvenient for layout optimization. A numerical model of the GaN transistor power loop inductance is essential.

A well-known low inductance power loop layout method is shown in Fig. 1(b). Magnetic cancellation is achieved by opposite current flows in the paralleled planes, which helps to reduce the power loop inductance [12]. To numerically quantify the power loop inductance value, the classic equation for PCB inductance calculation is generally used as

$$L_{pcb} = \mu_0 \frac{h}{w} l \ , \tag{1}$$

where μ_0 is the vacuum permeability, w is the conductor width, l is the conductor length and h is the vertical distance between the two conductors. The classic equation is derived from the Maxwell equation and Biot-Savart law, and simplified on the 2D geometry, as shown in Fig. 1(c), based on the assumption of uniform electric field (H field) between two infinite long tracks. However, the classic equation is reported to be inaccurate in low w/h ratios and a more complex numeric model is researched in [13]. The model is based on the premise of uniform current distribution within the two PCB tracks, which is not valid in the high frequency ringing scenarios.



(a) Power loop schematic

(b) Optimized PCB layout

(c) Cross section of PCB tracks

Fig. 1. GaN transistor totem pole.

The power loop inductance in the GaN transistor implementation is investigated in this paper. Section II explains several basic inductance concepts, and introduces how they matter in the power loop inductance modeling and quantification. The equivalent loop conductor concept is illustrated as a novel approach for power loop inductance quantification. In Section III, the numerical equation for power loop inductance estimation is provided based on the parameter sweep in FEA simulation, which is verified by the experimental results on the synchronous buck converter. Section IV concludes the paper.

II. Inductance in Transistor Power loop

A. Self-inductance and mutual-inductance

Inductance is one of the most widely misunderstood concepts in the electrical engineering [14]. As the basis for partial inductance and power loop inductance illustration, the fundamental concepts of inductance are first discussed. Alternating current in the conductor induces changing magnetic field (B), which is described by the Faraday's law shown in (2). Time-varying magnetic field cut through the closed loop conductor area will induce reverse voltage potential (ε) to oppose the original alternating current. Inductance is defined to describe this opposing relationship between the induced voltage potential and the original current. If the voltage potential is induced in the same conductor in which the alternating current is conducting, this effect is described as self-inductance (L). For the simplified 2D geometry conductor, the self-inductance is derived in (3) and defined as (4). It should be noted that a closed loop integration path has to be defined for both Faraday's law and inductance definition. In other words, the concept of inductance can only be applied in a closed loop conductor.

$$\oint \vec{E} \cdot dl = -\int \frac{\partial B}{\partial t} \cdot d\vec{S} \tag{2}$$

$$\varepsilon = -\frac{d}{dt} \iint \vec{B} \cdot d\vec{A} = -L\frac{di}{dt} \tag{3}$$

$$L = \frac{\iint \vec{B} \cdot d\vec{A}}{di} \tag{4}$$

The magnetic field induced by current can be calculated by Biot-Savart law, as shown in (5), where μ_0 is the vacuum permeability and r is the differential element in the direction of conventional current. According to (4) and (5), it should be noted that the self inductance is irrelevant to the amplitude and frequency of the excitation current.

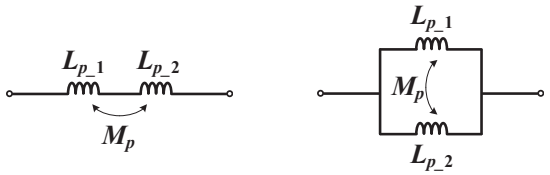
$$B_r = \frac{\mu_0}{4\pi} \int_C \frac{idl \times r'}{|r'|^3} \tag{5}$$

Mutual-inductance (M) is used to describe the effect when the opposing voltage potential is induced by the alternating current in another conductor, which is defined in (6) and (7). It should be noted that the mutual-inductance between two conductors are the same, which can be proved by Biot-Savart law and Ampere's circuital law. Mutual-inductance can be numerically calculated according to the coupling coefficient (K) and self-inductance of each conductors, as shown in 3. The coupling coefficient K varies from 0 to 1 and decided by the spatial alignment of the two conductors.

$$M_{12} = \frac{\iint \vec{B_{12}} \cdot d\vec{A_2}}{di_1} \tag{6}$$

$$M_{21} = \frac{\iint \vec{B_{21}} \cdot d\vec{A_1}}{di_2} \tag{7}$$

$$M_{12} = M_{21} = K \cdot \sqrt{L_1 L_2} \tag{8}$$



(a) Series connection. (b) Parallel connection.

Fig. 2. Series and parallel connection of partial inductance.

Several points need to be emphasized include:

(1) Inductance must be defined in a close loop conductor

(2) Self-inductance is decided by the current flow path and the space permeability.

(3) Mutual-inductance is defined in the geometry of two adjacent closed loop conductors.

(4) Mutual-inductance is decided by the current flow path in each conductor, spacial alignment of the two conductors and the space permeability.

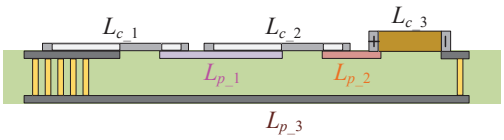
B. Partial-inductance

As discussed in the last section, self-inductance and mutual-inductance are used to investigate the electromagnetic interference (EMI) of and in between the close-loop conductors. However, in the research of high-speed digital circuit and long-distance transmission line, there's a growing interest in the electromagnetic induction of the partial element within a circuit operation. The concept of partial-inductance is thus proposed to break the total conductor loop into multiple elements and individually investigate the EMI between these elements. The inductance of via, wire or PCB tracks discussed in many books and papers are all within the scope of partial-inductance. Self-partial-inductance (L_p) and mutual-partial-inductance (M_p) are defined in a similar way as (3)(6)(7), numeral value of which are determined by the current distribution and spatial alignment of the partial branches. Parallel and series connection of partial inductance is shown in Fig. 2 and the corresponding numeral equation are shown in (9)(10).

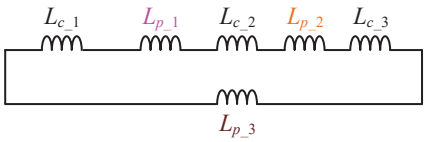
$$L_{p\_series} = L_{p\_1} + L_{p\_2} + 2M_p \tag{9}$$

$$L_{p\_parallel} = \frac{L_{p\_1}L_{p\_2} - M_p^2}{L_{p\_1} + L_{p\_2} - 2M_p} \tag{10}$$

Inductance of one single piece of copper cannot be defined without a ground path identified. Similarly, partial inductance itself doesn't have a physical meaning. Any numeral value of partial inductance from calculation, simulation or manufacturer data sheet is based on one assumed ground return path. However, partial inductance can be used to optimize the loop inductance. The overall inductance of a closed loop conductor can be obtained by summing up the partial inductance of each partial element according to (9). (10) reveals the EMI effect between the partial paralleled conductors, which is used in [6] for gate loop and power loop optimization.

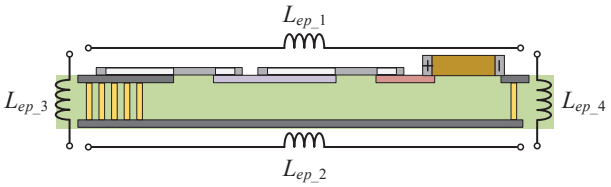


(a) Partial inductance network in PCB layout.

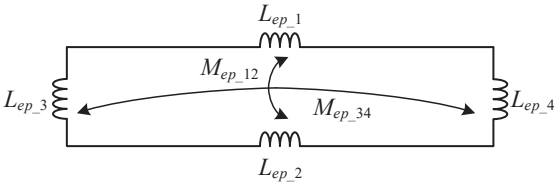


(b) Equivalent circuit.

Fig. 3. Partial inductance in power loop.



(a) Equivalent partial inductance network in PCB layout.



(b) Equivalent circuit.

Fig. 4. Equivalent power loop inductance.

C. Partial inductance in the converter power loop

The partial inductance network within a power loop can be given as the equivalent circuit shown in Fig. 3. L_{c_1}, L_{c_2} and L_{c_3} are the parasitic inductance from the package of GaN transistor and decoupling capacitor respectively. The chip scale package widely adopted by the GaN transistor manufacturers largely reduces this package inductance as low as 0.1 nH. L_{p_1}, L_{p_2} and L_{p_3} are the partial inductance from PCB tracks, which contribute to the majority of the power loop inductance. In addition to the self partial inductance, there's mutual partial inductance between each two conductor elements, which is omitted in Fig. 3(b) for simplicity. This model is the basis of 3D FEA simulation. FEA results can be obtained as a $m \times m$ matrix, where m pieces of conductors are considered in the simulation. Diagonal elements in the matrix can be explained as the self partial inductance and non-diagonal elements can be explained as the mutual partial inductance.

To simplify the close-geometry EMI interference between each PCB tracks, the equivalent partial inductance model is shown in Fig. 4. For the PCB layout with regular shaped PCB tracks, the partial inductance of two paralleled plates (L_{ep_1}, L_{ep_2} and M_{ep_12}) contributes to the majority of power loop inductance. Impact of the partial inductance L_{ep_1}, L_{ep_2} and M_{ep_12} is generally neglected. Instead of solving the partial self inductance and partial mutual inductance individually, the power loop inductance is estimated based on the magnetic flux and conduction current distribution. This model is generally used as the basis of 2D FEA simulation and numerical equation derivation.

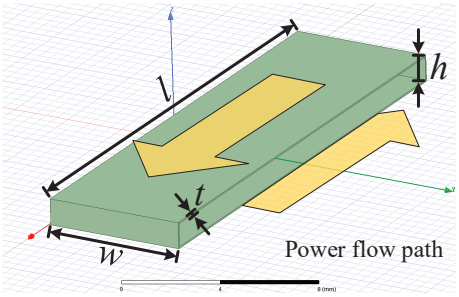


Fig. 5. Power loop equivalent conductor.

III. Numerical Quantification Based on the Loop Method

A. Loop Inductance Quantification

In this paper, the power loop inductance is further equivalent to the self inductance of one single equivalent inductor as shown in Fig. 5. The equivalent conductor has the same geometry dimensions as the PCB tracks in the layout method shown in Fig. 1(b). Numerical equation of the power loop inductance is obtained by the curve fitting of FEA results collected from the equivalent conductor parameter sweep. TABLE I shows the geometry values used in the parameter sweep, which is defined by the dimensions of the GaN transistor package and the decoupling capacitor package.

Inductance of the equivalent conductor can be viewed as proportional to the length l in the considered geometry range, which has been proved in prior-art numerical derivation. Copper thickness t has no impact on the inductance value for the proximity effect during the high frequency ringing. Parameter sweep range of h is decided by the general clearance between internal layers of PCB and the range of general PCB board thickness, which is collected from the PCB manufacturer. Parameter sweep range of w covers all the width value of commercial available GaN transistor package, which is

TABLE I
Geometry Values Used in the Parameter Sweep

Default parameter	h	w	l	t
	1 mm	6 mm	20 mm	0.07 mm
Parameter sweep	h		w	
	0.1 - 0.3 mm (0.05 mm spacing) 0.5 - 4 mm (0.5 mm spacing)		1 - 15 mm (1 mm spacing)	

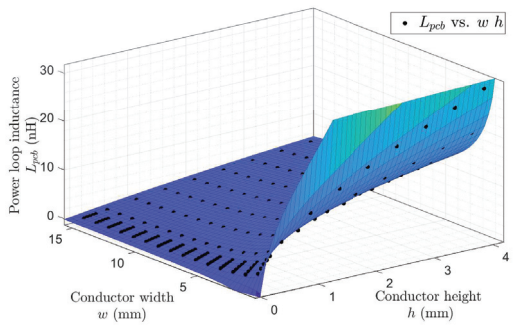


Fig. 6. Curve fitting of the FEA results given in MATLAB.

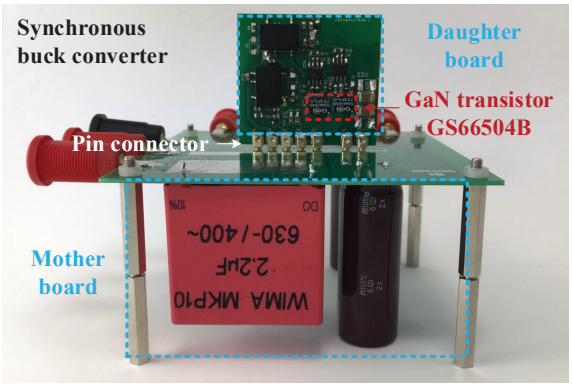


Fig. 7. Synchronous buck converter prototype.

collected from the GaN manufacturer data sheet. This method can be viewed as a trade-off between the time-consuming FEA simulation on the practical PCB tracks model and the mathematical derived equation with limited accuracy range. Benefit from the regular shape of the equivalent conductor, the FEA simulation model with user defined geometry parameters is easily built in ANSYS Maxwell. Computation load of the FEA parameter sweep is greatly lowered and 195 points of inductance value are obtained with 10 hours' simulation time on the laptop.

$$L_{loop} \cong \mu_0 \frac{h}{w} l\left(\frac{0.27}{1 - 0.74 \cdot e^{-0.45(h/w)}}\right) \tag{11}$$

The FEA simulation data is then imported into MATLAB. As shown in Fig. 6, curve fitting is done by the logistic correction on the classic equation (1). The customized power loop inductance equation is given as (11), which shows a high goodness of fit with R-square value equals 0.9992 (ideal fitting value is 1).

B. Experimental Validation

A synchronous buck converter is set up to validate the proposed numerical equation. As shown in Fig. 7, two GaN transistors (GS66504B) are configured as totem pole using the low inductance PCB layout. The duty ratio of synchronous buck converter is set to be 0.5 and first tested in 400 V, 300 W switching condition. As shown in Fig. 8, both high side

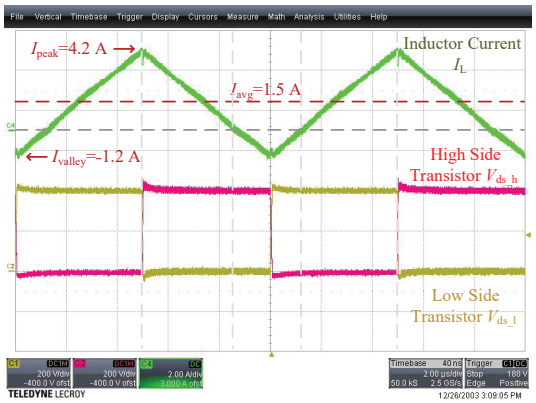


Fig. 8. Experimental waveform of the synchronous buck converter.

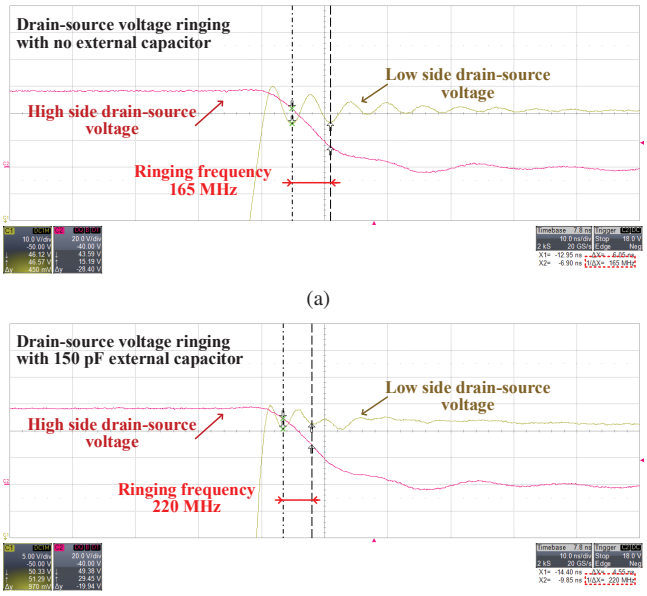


Fig. 9. Measured drain-source voltage ringing at 50 V DC bus.

and low side transistor shows a well switching performance with minor voltage ringing on the drain-source voltage.

$$f_0 = 1/2\pi\sqrt{L_{loop}C_{oss}} \tag{12}$$

$$f_1 = 1/2\pi\sqrt{L_{loop}(C_{oss} + C_{ex})} \tag{13}$$

To correctly obtain the power loop inductance in the prototype, drain-source voltage ringing frequency is measured. During the switching transient, the power loop inductance is resonant with the transistor output capacitor and the frequency can be obtained as (12). If external capacitor is paralleled to the transistor, the ringing frequency frequency will change to (13). By solving (12) and (13), power loop inductance L_{loop} and transistor output capacitance C_{oss} can thus be solved. In this test, the switching voltage is set to be 50 V. At this low drain-source voltage, C_{oss} is lowered to around 200 pF, while

TABLE II
COMPARISON OF THE POWER LOOP INDUCTANCE ESTIMATION METHOD

Measured data f_0=165 MHz f_1=220 MHz	Estimation value based on (12) (13) C_{oss} = 192.9pF L_{loop} = 2.7 nH
Geometry data l = 17 mm w = 6 mm h = 0.95 mm	Estimation value based on the classic equation (1) L_{loop} = 3.4 nH
	Estimation value based on the proposed equation (11) L_{loop} = 2.9 nH

the power loop inductance is not relevant to the conduction current density. Therefore, the ringing frequency is lowered below 300 MHz, which is within the bandwidth of general passive voltage probe. External capacitor is selected to be close to the transistor output capacitance value (150 pF used in this test), which guarantees the measurement accuracy. The obtained ringing waveform is shown in Fig. 9.

Estimation of the power loop inductance is summarized in TABLE II. From the measured ringing frequency, the power loop inductance is estimated to be 2.7 nH according to (12) (13). This value is corroborated by the estimated transistor C_{oss} value, which fits the characterization curve specified in the data sheet. Using the proposed numerical equation, the estimation value based on the layout geometry data is only 0.2 nH larger than the estimation value from the experimental results. The proposed method shows a high estimation accuracy with the deviation rate of 7 %, which is much smaller than the 26 % deviation rate by the classic equation.

IV. CONCLUSION

In this paper, power loop inductance in the GaN transistor PCB layout is discussed. The basic concepts of self, mutual and partial inductance, and their impact on the power loop inductance quantification are illustrated. A numerical equation for the GaN transistor power loop inductance estimation is given based on the FEA results of the loop conductor parameter sweep. The proposed method shows a high estimation accuracy compared with the experimental results from the synchronous buck converter.

REFERENCES

[1] M. Danilovic, Z. Chen, R. Wang, F. Luo, D. Boroyevich, and P. Mattavelli, "Evaluation of the switching characteristics of a gallium-nitride transistor," *IEEE Energy Conversion Congress and Exposition: Energy Conversion Innovation for a Clean Energy Future, ECCE 2011, Proceedings*, pp. 2681–2688, 2011.

[2] J. Lautner and B. Piepenbreier, "Analysis of GaN HEMT switching behavior," *9th International Conference on Power Electronics - ECCE Asia: "Green World with Power Electronics", ICPE 2015-ECCE Asia*, pp. 567–574, 2015.

[3] H. Li, X. Li, Z. Zhang, C. Yao, and J. Wang, "Design consideration of high power GaN inverter," *WiPDA 2016 - 4th IEEE Workshop on Wide Bandgap Power Devices and Applications*, pp. 23–29, 2016.

[4] B. Sun, R. Burgos, X. Zhang, and D. Boroyevich, "Active dv/dt control of 600V GaN transistors," in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*. IEEE, sep 2016, pp. 1–8.

[5] Z. L. Zhang, Z. Dong, X. W. Zou, and X. Ren, "A Digital Adaptive Driving Scheme for eGaN HEMTs in VHF Converters," *IEEE Transactions on Power Electronics*, vol. 32, no. 8, pp. 6197–6205, 2017.

[6] K. Wang, L. Wang, X. Yang, X. Zeng, W. Chen, and H. Li, "A Multiloop Method for Minimization of Parasitic Inductance in GaN-Based High-Frequency DC-DC Converter," *IEEE Transactions on Power Electronics*, vol. 32, no. 6, pp. 4728–4740, 2017.

[7] Z. Liu, X. Huang, F. C. Lee, and Q. Li, "Package parasitic inductance extraction and simulation model development for the high-voltage cascode GaN HEMT," *IEEE Transactions on Power Electronics*, vol. 29, no. 4, pp. 1977–1985, 2014.

[8] W. Zhang, X. Huang, F. C. Lee, and Q. Li, "Gate drive design considerations for high voltage cascode GaN HEMT," *Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC*, pp. 1484–1489, 2014.

[9] R. Hou, J. Lu, and D. Chen, "Parasitic capacitance Eqoss loss mechanism, calculation, and measurement in hard-switching for GaN HEMTs," *Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC*, vol. 2018-March, pp. 919–924, 2018.

[10] A. B. Jorgensen, S. Beczkowski, C. Uhrenfeldt, N. H. Petersen, S. Jorgensen, and S. Munk-Nielsen, "A Fast-Switching Integrated Full-Bridge Power Module Based on GaN eHEMT Devices," *IEEE Transactions on Power Electronics*, vol. 1, no. c, 2018.

[11] B. Zhao and X. Zhang, "An Efficiency-oriented Two-stage Optimal Design Methodology of High Frequency LCLC Resonant Converters for Space Travelling-Wave Tube Amplifier Applications," *IEEE Transactions on Industrial Electronics*, vol. PP, no. c, pp. 1–1, 2019.

[12] D. Reusch and J. Strydom, "Understanding the effect of PCB layout on circuit performance in a high frequency gallium nitride based point of load converter," *IEEE Transactions on Power Electronics*, vol. PP, no. 99, p. 1, 2013.

[13] A. Letellier, M. Dubois, J. P. F. Trovao, and H. Maher, "Calculation of PCB Power Loop Stray Inductance in GaN or High di/dt Applications," *IEEE Transactions on Power Electronics*, vol. 8993, no. c, p. 1, 2018.

[14] B. Archambeault, "Inductance and Partial Inductance What's it all mean ?" *IEE EMC Society Newsletter*, vol. Winter, no. 224, 2010.